

Analog & Mixed-Signal Integrated Circuit Design: Fundamentals, Simulation, and Layout

The semiconductor industry is experiencing rapid growth, with companies investing heavily. However, the significant shortage of skilled and highly educated workers in North America raises concerns about the industry's ability to sustain this growth. Addressing this workforce gap requires attracting students to the chip design field and providing specialized training programs tailored to the semiconductor ecosystem.

The 2nd Canadian Bootcamp on Analog and Mixed-Signal Integrated Circuits (ICs) is designed to support this effort by providing targeted training and upskilling opportunities for engineers and graduate students. The program consists of five full days of lectures and hands-on exercises, organized into two parallel tracks, led by leading academic and industry experts, including instructors from McGill University, Concordia University, Université du Québec à Montréal, and industry leaders from Cadence Design Systems and CoMeT-IC Consulting.

In one track, participants will gain knowledge in analog and mixed-signal IC design, including CMOS operational amplifier design, Sigma-Delta converters, phase-locked loops, CMOS layout techniques, standard cell development, and bandgap reference circuits. In a second track, participants will be introduced to the fundamental of IC design for wireline communication, including high-speed latches, sense-amplifiers, serializers, transmitter and receiver circuits as well as equalizers equalizers. The program emphasizes practical learning, with each day consisting of three hours of lectures followed by three hours of guided hands-on design exercises.

This bootcamp benefits the semiconductor industry by upskilling current engineers and providing networking opportunities with potential employees and interns. Graduate students will also gain access to practical IC design and layout training that may not be available at their home institutions.

The bootcamp will be held in person at the Université du Québec à Montréal campus in downtown Montreal, Canada, from Monday, May 11, to Friday, May 15, 2026. The program will host up to 40 participants, including 15 industry professionals and 25 graduate students.

Registration and more info at <https://sites.grenadine.uqam.ca/sites/facultesciences/en/2ndams/>

Bootcamp Q&A and summary:

When will it take place?

May 11th (Monday) to May 15th (Friday)

Where will it be held?

In-person in Montreal, QC, Canada (downtown)

How Much does it cost?

The registration fees include breakfast, lunch, etc. (except dinner)

Graduate students: \$1250 CAD

Industry guests: \$2850 CAD

Who should attend it?

Twenty-five (25) graduate students interested in gaining practical expertise in high-speed analog and mixed-signal integrated circuit design. Fifteen (15) industry professionals with prior IC design experience seeking advanced training, upskilling, or professional requalification

Can I cancel after registration?

All cancellation requests must be submitted in writing no later than three (3) weeks prior to the event start date to qualify for a full refund of the registration fee, less \$200. Cancellation requests received after this deadline will not be eligible for a full refund.

The organizers assume no responsibility for travel, accommodation, or related expenses and do not guarantee reimbursement of such costs under any circumstances.

Could this event be canceled?

The organizers reserve the right to cancel the event if a sufficient number of participants is not registered. In the event of cancellation, all registered participants will be notified no later than April 20, 2026 and fully refunded.

How can I register? Please go to <https://sites.grenadine.uqam.ca/sites/facultesciences/en/2ndams/>

What are the pre-requisites?

Participants should possess foundational knowledge of transistor-level integrated circuit design and be familiar with industry-standard EDA tools, including Cadence and Synopsys. Each attendee is required to bring a personal laptop to support participation in practical exercises and design sessions.

What will be taught and who will be the instructors?

Tutorial #1 (Day 1 & 2): Fundamentals of analog & mixed-signal ICs design, Gordon W. Roberts, McGill University, <https://www.ece.mcgill.ca/~grober4/ROBERTS/Welcome.html> (2 half days theory and 2 half days hands-on design experience) focused on:

- Linear and nonlinear system behavior
- Analog and mixed-signal basics building blocks
- Manufacturing concerns
- Principles of feedback and its applications to CMOS Opamp design and simulation
- Data conversion using Sigma-Delta Modulators, and Phase-Locked-Loop (if time permits)

Tutorial #2 (Day 3 & 4): Introduction to CMOS layout design and development of standard cells for mixed-signal design, Dan Clein <https://www.comet-ic.com/> , <https://www.theunorthodoxmanager.com/> (2 half-days theory, and 2 half-days layout implementation):

- What is CMOS VLSI Layout?
- What are the quality metrics for layout design in general?
- Where can analog/RF take advantage of cell libraries and why?
- How to build a standard cell library for digital and for mixed signal (similarities and differences)

Tutorial #3 (Day 5): Low-Voltage CMOS Reference Circuits: Fundamentals, design, and simulation, Christian Fayomi, UQAM <https://professeurs.uqam.ca/professeur/fayomi.c/>, (half-day theory, and half-day implementation):

- Bandgap reference fundamentals
- Simplest bandgap references
- Case study: design and characterization of a bandgap reference using 45 nm CMOS

Tutorial # 4: High-Speed Wireline Communications: Introduction, fundamentals, and advanced topics
Day 1 & 3: High-Speed Wireline Circuits, Glenn Cowan, Concordia University <https://users.encs.concordia.ca/~gcowan/>, (2 half-days theory and 2 half-days hands-on design experience):

- Introduction to wireline communication
- Fundamentals of equalization
- CML circuits for transmitter and receiver equalizers
- Inverter-based circuits for transmitters

Day 2, 4 & 5: High-Speed Wireline Circuits, Michael Venditti, Design Engineering Director at Cadence and Louis-Francois Tanguay, Sr Principal Design Engineer at Cadence (3 half-days theory and 3 half-days hands-on design experience):

- Sense amplifiers and clocking
- Serializers
- Advanced topics: tips and tricks for efficient simulation
- Design partitioning, Intro to advanced wireline topics.

Technology (Cadence tools and process): CMOS 45 nm generic process

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